Listing of Claims:

1. (Currently Amended) A process for writing data into registers of at least one device ~~(4)~~ comprising a management interface ~~(6)~~, ~~characterised by the following~~ comprising the steps of:

[[-]] composing ATM cells ~~by~~ via at least one management unit ~~(1)~~, ~~with the~~ said management unit ~~(1)~~ addressing ~~the~~ each ATM cell ~~cells in each instance~~ to a control unit ~~(5)~~ linked to a data path interface [[(7),]] and ~~integration of~~ integrating instructions associated with particular devices [[(4),]] ~~e.g. writing of data into the registers of the devices (4), in the form of an operation code,~~ together with ~~the~~ respective information into ~~the~~ a payload of the ATM cells;

[[-]] transmitting ~~the~~ ATM cells to the addressed control unit ~~(5)~~ via ~~the~~ a respective data path interface ~~(7)~~;

[[-]] extracting ~~the~~ operation codes ~~being~~ associated with particular devices ~~(4)~~, ~~and the~~ associated information being contained in the payload of the ATM cells in the control unit ~~(5) contained in the payload of the ATM cell~~; and

[[-]] ~~if after the operation code, data is to be entered, setting of the register values of the devices (4) according to the information provided from the ATM cell for this~~

setting the register values of the devices ~~(4)~~ according to the information provided from the ATM cell if data is to be entered after the operation codes are extracted;

wherein for each ATM cell to be composed, the control unit maps a current interrupt state of the connected devices into interrupt bits which are provided in the payload of the ATM cells.

2. (Currently Amended) A process for reading values from registers of a device ~~(4)~~ comprising a management interface, ~~(6) characterised by the following~~ comprising the steps of:

[[-]] composing ATM cells ~~by~~ via at least one management unit ~~(1)~~, ~~with the~~ said management unit ~~(1)~~ addressing ~~the~~ each ATM cell ~~cells in each instance~~ to a control unit ~~(5)~~ linked to a data path interface ~~(7)~~, and integrating

instructions associated with particular devices ~~(4), e.g. reading of data from the registers of the devices (4), in the form of an operation code,~~ together with ~~the~~ respective information into the payload of ~~the~~ ATM cells;

[[-]] transmitting the ATM cells to the addressed control unit ~~(5)~~ via the respective data path interface ~~(7);~~,

[[-]] extracting the operation codes being associated with particular devices [[(4),]] and the associated information ~~in the control unit (5)~~ contained in the payload of ~~the~~ each ATM cell in the control unit; and

[[-]] ~~if after the operation code, register values are to be read out from devices (4),~~ reading ~~of the~~ register values of the respective devices ~~(4)~~, if after the operation codes are extracted, register values are to be read out from devices;

wherein ~~integration of~~ the read values are integrated into ATM cells ~~with addressing~~ which addressed to the management unit ~~(1)~~ and ~~transmission of the cells~~ transmitted to the management unit, and for each ATM cell to be composed, the control unit maps a current interrupt state of the connected devices into interrupt bits which are provided in the payload of the ATM cells.

3. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 1, ~~characterised in that~~ wherein the devices ~~(4)~~ are ATM interface units of the physical layer by ~~means of~~ which a data path interface ~~(7)~~ provides ~~access for~~ the ATM layer with access to a physical transmission medium.

4. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 1, ~~characterised in that~~ wherein addressing of ATM cells to the control unit ~~(5)~~ by the management unit ~~(1) takes place~~ occurs via a VPI/VCI address associated with the control unit ~~(5)~~, or via a reserved UTOPIA bus address of the data interface if the management unit ~~(1)~~ communicates directly with the control unit [[(5),]] via an UTOPIA data interface ~~(7), addressing takes place via a reserved UTOPIA bus address of the data interface (7)~~.

5. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 1, ~~characterised in that~~ wherein addressing of ATM cells to the management unit ~~(1)~~ by the control unit ~~(5) takes place~~ occurs via a VPI/VCI address associated with the management unit ~~(1)~~, or via a reserved UTOPIA bus address of the data interface if the management unit ~~(1)~~ communicates directly with the control unit [[(5),]] via a UTOPIA data interface ~~(7), addressing takes place via a reserved UTOPIA bus address of the data interface (7)~~.

6. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 1, ~~characterised in that~~ wherein transmission of the ATM cells is based on ~~the~~ a request-response protocol.

7. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 6, ~~characterised in that~~ wherein the management unit ~~(1) does not send any further~~ refrains from sending additional ATM cells to a control unit ~~(5) as long as it has not received~~ until a correct response to ~~the~~ a preceding ATM cell from said control unit is received by the management unit [[(5),]] ~~or as long as a~~ or until a time limit ~~has not been~~ is exceeded.

8. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 1, ~~characterised in that~~ wherein prior to any forwarding of ATM cells destined for the management unit ~~(1)~~, the control unit ~~(5)~~ forms a checksum, and prior to any forwarding of ATM cells destined for a control unit ~~(5)~~, the management unit ~~(1)~~ forms a checksum, across at least part of the payload of the ATM cell and integrates this sum into the ATM cell to be transmitted.

9. (Currently Amended) ~~A~~ The process according to claim 1, ~~characterised in that~~ wherein prior to ~~carrying out~~ performing any instructions, the control unit ~~(5)~~ checks a checksum transmitted with the received ATM cell ~~received~~, and ~~carries out~~ performs the instructions only if no transmission error is detected[[;]], otherwise ~~it~~ the control unit discards the ATM cell and is ready to receive new ATM cells.

10. (Currently Amended) ~~A~~ The process according to claim 9, ~~characterised in that~~ wherein after ~~each~~ processing ~~of the instructions~~ each instruction of an ATM cell, the control unit ~~(5)~~ places at least part of ~~the~~ updated content of the ATM cell to be transmitted to a

management unit~~, in particular the updated content of the entire cell,~~ into an intermediate memory.

11. (Currently Amended) ~~A~~ The process according to claim 8, ~~characterised in that~~ wherein [[-]] after a specified time limit after sending a first ATM cell addressed to a control unit ~~(5)~~ has lapsed and prior to receiving a response ATM cell from the control unit ~~(5)~~ with a correct CRC sum, the management unit ~~(1)~~ resends ~~sends the same~~ an identical ATM cell ~~again, identifying it~~ the ATM cell as a repetition cell[[; -]], when receiving a repetition cell, the control unit ~~(5)~~ checks whether ~~or not~~, following ~~the~~ a first ATM cell, a response ATM cell was transmitted to the management unit [[(1);]], and [[-]] if a response ATM cell call was not transmitted to the management unit ~~no~~, the control unit processes the instructions contained in the cell[[;]], or [[-]] if a response ATM cell was transmitted to the management unit ~~yes~~, the control unit retransmits the response ATM cell which was previously ~~has already been~~ sent once and ~~which has been~~ stored separately[[,]] to the management unit ~~(1)~~.

12. (Canceled)

13. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 1, ~~characterised in that~~ wherein the control unit ~~(5)~~ autonomously and regularly reads in data from devices ~~(4)~~ connected to ~~it~~ the control unit and transmits ~~such~~ the data, integrated into ATM cells, to the management unit ~~(1)~~.

14. (Currently Amended) A control unit ~~(5)~~ providing access to ~~the~~ a management interface ~~(1)~~ of at least one device ~~(4)~~ comprising registers as well as to a data path interface ~~(7)~~ of an ATM network, [with the] said control unit ~~(5)~~ being configured to ~~suitable for receiving~~ receive ATM cells composed by a management unit ~~(1)~~ and destined for the control unit ~~(5)~~ via the data path interface ~~(7)~~, and ~~extracting and carrying out~~ being configured to extract individual instructions associated with a particular device from a payload of the devices ~~(4), in particular reading and/or writing of register data into the devices (4) or from the devices (4) from the payload of these cells~~ and ~~extracting them and carrying them out in~~ extract and perform the individual instructions associated ~~respect of the~~ with a respective device ~~(4)~~;

wherein for each ATM cell to composed, the control unit maps the current interrupt state of the connected devices into interrupt bits provided for this purpose in the payload of the ATM cell.

15. (Currently Amended) ~~A~~ The control unit ~~(5) according to~~ of claim 14, ~~characterised in that~~ wherein the management interface ~~(6) corresponds to~~ is the management interface as proposed in Appendix 2 of Utopia Level 2 specification.

16. (Currently Amended) ~~A~~ The control unit ~~(5) according to~~ of claim 14, ~~characterised in that~~ wherein the data path interface ~~(7) corresponds to the~~ is the data path interface as specified in Appendix 2 of Utopia Level 2 specification.

17. (Currently Amended) ~~A~~ The control unit ~~(5) according to~~ of claim 14, ~~characterised in that~~ wherein the control unit is configured to compose it is ~~suitable for composing~~ the register data read from the registers of the devices ~~(4)~~ to ~~become~~ ATM cells, address ~~it~~ the ATM cells to a management unit ~~(1) by means of~~ via the VPI/VCI address of the management unit [[(1),]] or address ~~it~~ the ATM cells using a UTOPIA address reserved for inband communication, and forward ~~it~~ the ATM cells to the data path interface ~~(7)~~.

18. (Currently Amended) ~~A~~ The control unit ~~(5) according to~~ of claim 17, ~~characterised in that it~~ wherein the control unit comprises an intermediate memory for storing at least part of the content of the ATM cell to be transmitted to the management unit ~~(1)~~.

19. (Currently Amended) ~~A~~ The management system for an ATM network for at least one of configuring and ~~and/or~~ monitoring devices ~~(4)~~ comprising registers and a management interface ~~(6)~~, respectively, with the management system comprising control units ~~(5)~~ according to claim ~~one of claims~~ 14 [[-]] ~~18~~, as well as at least one management unit ~~(1) suitable for generating~~ configured to generate configuration data for the devices ~~(4) and/or for processing the~~ and process data available from ~~the~~ registers of the devices ~~(4), with the~~, said management unit ~~(1)~~ being ~~suitable for generating~~ configured to respectively generate instructions for a particular device ~~(4) respectively~~, for joining instructions and data for one or several devices ~~(4)~~ to which

an identical ~~the same~~ control unit ~~(5)~~ has access, as a payload of an ATM cell and for addressing the ATM cell to the respective control unit ~~(5)~~.

20. (Currently Amended) ~~A~~ The management system ~~according to~~ of claim 19, ~~characterised in that~~ wherein the devices ~~(4)~~ comprising registers are connected to a unit of an ~~the~~ ATM layer of the ATM network via ~~the~~ a data path interface ~~(7)~~.

21. (Currently Amended) ~~A~~ The management system ~~according to~~ of claim 19, ~~characterised in that~~ wherein the devices ~~(4)~~ comprising registers are ATM interface units of ~~the~~ a physical layer ~~by way of~~ via which ~~the~~ an ATM layer of the ATM network has access to at least one transmission medium.

22. (Currently Amended) ~~A~~ The management system according to claim 21, ~~characterised in that~~ wherein the control unit ~~(5)~~ has access to management interfaces ~~(6)~~ of up to 31 interface units ~~(4)~~.

23. (Currently Amended) An ATM cell, comprising:

a cell header of 5 bytes and a payload space of 48 bytes, said cell being ~~used for transmitting~~ configured to transmit management data between a management unit ~~(1) with~~ having access to an ATM network and at least one device ~~(4)~~, ~~with~~ said device ~~(4)~~ comprising registers into which data is at least one of ~~to be written and/or from which data is to be~~ written and read out[[,]]; and

a management interface ~~(6) by way of~~ via which a control unit ~~(5)~~ has access to the registers of the device ~~(4)~~, said data being destined for the control unit, ~~with the~~ said control unit ~~(5) furthermore~~ also having access to a data path interface ~~(7)~~ of an ATM network[[,]] and being ~~suitable for receiving certain~~ configured to receive ATM cells composed by a management unit ~~(1)~~ via the data path interface ~~(7)~~[[,]] ~~said data being destined for the control unit (5)~~, ~~and~~ extract individual instructions associated with a particular device from ~~the~~ a payload space of ~~these~~ the ATM cells ~~to extract individual instructions associated with a particular device (4)~~[[,]] and extract associated information and perform instructions with respect to the particular device ~~in particular reading and/or~~

~~writing of register data into the devices (4) or from the devices (4), and to extract associated information and carry it out in respect of the particular device (4)~~[[,]]];

wherein ~~with~~ the payload space of the ATM cell ~~comprising~~ comprises instruction blocks in which respective bits, which are associated with particular registers integrated in the identified device, are provided [[-]] for an operation code which identifies an instruction type ~~such as read, write, no operation~~[[; -]] for identification of a device ~~(4)~~ to which ~~the~~ an instruction in ~~the~~ an instruction block is directed[[; -]] ~~which are associated with particular registers integrated in the identified device (4)~~[[;]], and [[-]] for data required for ~~carrying out~~ performing the instruction, and a supplementary block ~~(trailer)~~, in which bits are provided [[-]] for identifying the cell type[[,]] ~~such as new cell or a retransmitted cell~~[[; -]] as a sequential bit which is toggled with each composition of a new cell which does not constitute a repetition[[; -]] for interrupt information[[;]] and ~~as well as~~ [[-]] for a checksum;

wherein 11 instruction blocks and a supplementary block of 4 bytes each are used in each payload space, and 2 bits for the identification code, 3 - 5 bits for identification of the device, 0 - 2 bits in reserve for supplementing the instruction bit up to 5 bits, 17 bits for allocation of the registers, and 1 byte for data required to perform a respective instruction are provided for each of the 11 instruction blocks; and

wherein 1 bit for identification of the cell type, 1 bit as a sequential bit, 5 additional reserve bits, 1 byte for interrupt information, and 10 bits for the checksum, formed by a cyclic redundancy check (CRC), are each provided for the supplementary block.

24. (Canceled)

25. (Canceled)

26. (Currently Amended) ~~An~~ The ATM cell ~~according to~~ of claim 23, ~~characterised in that~~ wherein a "big endian order" is used for the ATM cell.

27. (Currently Amended) A method for constructing an ATM cell comprising a cell

header of 5 bytes and a payload space of 48 bytes, said ATM cell being ~~used for transmitting~~ configured to transmit management data between a management unit ~~(1) with~~ having access to an ATM network and at least one device ~~(4)~~, ~~with~~ said device ~~(4)~~ comprising registers into which data is ~~to be written and/or from which data is to be~~ at least one of written and read out, and a management interface ~~(6) by way of~~ via which a control unit ~~(5)~~ has access to the registers of the device ~~(4)~~, ~~with the~~ said data being designated for the control unit, said control unit ~~(5)~~ ~~furthermore~~ also having access to a data path interface ~~(7)~~ of ~~an~~ the ATM network, and being ~~suitable for receiving certain~~ configured to receive specific ATM cells composed by ~~a~~ the management unit ~~(1)~~ via the data path interface ~~(7)~~, ~~said data being designated for the control unit (5), and~~ extract individual instructions associated with a particular device from ~~the~~ a payload space of ~~these~~ the ATM cells and extract associated information and perform instructions with respect to the particular device ~~to extract individual instructions associated with a particular device (4), in particular reading and/or writing of register data into the devices (4) or from the devices (4), and to extract associated information and carry it out in respect of the particular device (4), with the~~, said payload space of the ATM cells ~~cell~~ comprising instruction blocks and a supplementary block ~~(trailer)~~, the method comprising the steps of:

[[-]] inserting into the instruction blocks bits for an operation code which identifies an instruction type ~~such as read, write, no operation~~;

[[-]] inserting into the instruction block bits for identification of the device ~~(4)~~ to which the instruction in the instruction block is directed;

[[-]] inserting into the instruction blocks bits which are associated with particular registers integrated in the identified device ~~(4)~~;

[[-]] inserting into the instruction blocks bits for data required for carrying out the instruction[[,]];

[[-]] inserting into the supplementary block bits for identifying the cell type[[,]] ~~such as new cell or a retransmitted cell~~;

[[-]] inserting into the supplementary block a sequential bit which is toggled with each composition of a new cell which does not constitute a repetition;

[[-]] inserting into the supplementary block bits for interrupt information; and

[[-]] inserting ~~in~~ into the supplementary block bits for a checksum;

wherein 11 instruction blocks and a supplementary block of 4 bytes each are used in each payload space for inserting the bits, and 2 bits for the operation code, 3-5 bits for identification of the device, 0-2 bits in reserve for supplementing the identification bits up to 5 bits, 17 bits for allocation of the registers, and 1 byte for the data required to perform a respective instruction are each inserted into the 11 instruction blocks; and

wherein 1 bit for identification of the cell type, 1 bit as a sequential bit, 5 bits additionally as a reserve, 1 byte for the interrupt information, and 10 bits for the checksum, formed by a cyclic redundancy check (CRC), are each inserted into the supplementary block.

28. (Canceled).

29. (Canceled)

30. (Currently Amended) A method according to claim 27, ~~characterised in that~~ wherein a "big endian order" is used for the ATM cells ~~cell~~.

31. (Currently Amended) A management unit for constructing an ATM cell, comprising:

a cell header of 5 bytes and a payload space of 48 bytes, said cell being ~~used for transmitting~~ configured to transmit management data between said management unit ~~(1)~~ with access to an ATM network and at least one device ~~(4)~~, said data being destined for the control unit, ~~with~~ said device ~~(4)~~ comprising registers into which data is ~~to be written and/or from which data is to be~~ at least one of written and read out[[,]]; and

a management interface ~~(6) by way of~~ via which a control unit ~~(5)~~ has access to the registers of the device ~~(4)~~, ~~with the~~ said control unit ~~(5) furthermore~~ also having access to a data path interface ~~(7)~~ of an ATM network, and being ~~suitable for receiving certain~~ configured to receive specific ATM cells composed by a management unit ~~(1)~~ via the data path interface ~~(7)~~, ~~said data being destined for the control unit (5)~~, and extract particular information associated with a

particular device from ~~the~~ a payload space of ~~these~~ the ATM cells ~~to extract individual instructions associated with a particular device (4), in particular reading and/or writing of register data into the devices (4) or from the devices (4), and to extract associated information and carry it out in respect of the particular device (4)~~, ~~with the~~ said payload space of the ATM cells ~~cell~~ comprising instruction blocks and a supplementary block ~~(trailer)~~[[,]] ;

wherein the management unit ~~(1) comprising~~ comprises means for [[: -]] inserting into the instruction blocks bits for an operation code which identifies an instruction type ~~such as read, write, no operation;~~, [[-]] inserting into the instruction blocks bits for identification of ~~a~~ the device ~~(4)~~ to which the instruction in the instruction block is directed[[; -]], inserting into the instruction blocks bits which are associated with particular registers integrated in the identified device (4)[[; -]], inserting into the instruction blocks bits for data required for ~~carrying out~~ performing the instruction[[; -]], inserting into the supplementary block bits for identifying the cell type~~, such as new cell or a retransmitted cell~~[[; -]], inserting into the supplementary block a sequential bit which is toggled with each composition of a new cell which does not constitute a repetition[[; -]], inserting into the supplementary block bits for interrupt information; and ~~for~~ [[-]] inserting into the supplementary block bits for a checksum;

wherein said means are arranged to insert 2 bits for the operation code, 3 - 5 bits for identification of the device, 0 - 2 bits in reserve for supplementing the instruction bit up to 5 bits, 17 bits for allocation of the registers, 1 byte for data required to perform a respective instruction into the 11 instruction blocks; and

wherein said means are arranged to insert 1 bit for identification of the cell type, 1 bit as a sequential bit, 5 additional reserve bits, 1 byte for the interrupt information, and 10 bits for the checksum, formed by a cyclic redundancy check (CRC), into the supplementary block.

32. (Canceled)

33. (Canceled)

34. (Currently Amended) The Management unit ~~according to~~ of claim 31, ~~characterized in that~~ wherein the means are ~~suited for using~~ use a "big endian order".

35. Currently Amended) The ~~use of an~~ ATM cell ~~according to~~ of claim 23, ~~for configuring~~ wherein the ATM cell configures ATM interface units ~~(4)~~ of ~~the~~ a physical layer.

36. (Currently Amended) The ~~use of an~~ ATM cell ~~according to~~ claim 23 ~~for~~ wherein the ATM cell ~~the reading~~ reads out ~~of~~ data which is available in ~~the~~ ATM interface units ~~(4)~~ of ~~the~~ a physical layer.

37. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 2, ~~characterised in that~~ wherein the devices ~~(4)~~ are ATM interface units of ~~the~~ a physical layer by ~~means of~~ which a data path interface ~~(7)~~ provides access for ~~the~~ ATM layer to a physical transmission medium.

38. (Currently Amended) ~~A process according to~~ The process of claim 2, ~~characterised in that~~ wherein addressing of ATM cells to the control unit ~~(5)~~ by the management unit ~~(1) takes place~~ occurs via a VPI/VCI address associated with the control unit ~~(5)~~[[,]] or ~~if the management unit (1) communicates directly with the control unit (5), via an UTOPIA data interface (7), addressing takes place~~ via a reserved UTOPIA bus address of the data interface ~~(7)~~ if the management unit communicates directly with the control unit via an UTOPIA data interface.

39. (Currently Amended) ~~A process according to~~ The process of claim 2, ~~characterised in that~~ wherein addressing of ATM cells to the management unit ~~(1)~~ by the control unit ~~(5) takes place~~ occurs via a VPI/VCI address associated with the management unit ~~(1)~~[[,]] or via a reserved UTOPIA bus address of the data interface if the management unit ~~(1)~~ communicates directly with the control unit [[(5),]] via a UTOPIA data interface [[(7),]] ~~addressing takes place via a reserved UTOPIA bus address of the data interface (7)~~.

40. (Currently Amended) ~~A process according to~~ The process of claim 2, ~~characterised in~~

~~that~~ wherein transmission of the ATM cells is based on ~~the~~ a request-response protocol.

41. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 40, ~~characterised in that~~ wherein the management unit ~~(1) does not send any further~~ refrains from sending additional ATM cells to a control unit ~~(5) as long as it has not received~~ until a correct response to ~~the~~ a preceding ATM cell from said control unit is received by the management unit ~~(5)~~, ~~or as long as~~ a or until a time limit ~~has not been~~ is exceeded.

42. (Currently Amended) ~~A~~ The process ~~according to~~ of claim 2, ~~characterised in that~~ wherein prior to any forwarding of ATM cells destined for the management unit ~~(1)~~, the control unit ~~(5)~~ forms a checksum, and prior to any forwarding of ATM cells destined for a control unit ~~(5)~~, the management unit ~~(1)~~ forms a checksum, across at least part of the payload of the ATM cell and integrates this sum into the ATM cell to be transmitted.

43. (Currently Amended) ~~A~~ The process according to claim 2, ~~characterised in that~~ wherein prior to ~~carrying out~~ performing any instructions, the control unit ~~(5)~~ checks a checksum transmitted with the received ATM cell ~~received~~, and ~~carries out~~ performs the instructions only if no transmission error is detected; otherwise ~~it~~ the control unit discards the ATM cell and is ready to receive new ATM cells.

44. (Currently Amended) ~~A~~ The process according to claim 43, ~~characterised in that~~ wherein after each processing ~~of the~~ instructions of an ATM cell, the control unit ~~(5)~~ places at least part of ~~the~~ updated content of the ATM cell to be transmitted to a management unit~~, in particular the updated content of the entire cell,~~ into an intermediate memory.

45. (Currently Amended) ~~A~~ The process according to claim 42, ~~characterised in that~~ wherein [[-]] after a specified time limit after sending a first ATM cell addressed to a control unit ~~(5)~~ has lapsed and prior to receiving a response ATM cell from the control unit ~~(5)~~ with a correct CRC sum, the management unit ~~(1)~~ resends ~~sends the same~~ an identical ATM cell ~~again, identifying it~~ the ATM cell as a repetition cell[[; -]], when receiving a repetition cell, the control unit ~~(5)~~ checks whether ~~or not~~, following ~~the~~ a first ATM cell, a response ATM cell was

transmitted to the management unit [[(1);]], and [[-]] if a response ATM cell call was not transmitted to the management unit ~~no~~, the control unit processes the instructions contained in the cell[[;]], or [[-]] if a response ATM cell was transmitted to the management unit ~~yes~~, the control unit retransmits the response ATM cell which was previously ~~has already been~~ sent once and ~~which has been~~ stored separately[[,]] to the management unit ~~(1)~~.

46. (Currently Amended) ~~A~~ The process according to claim 9, ~~characterised in that~~ wherein[[-]] after a specified time limit after sending a first ATM cell addressed to a control unit ~~(5)~~has lapsed and prior to receiving a response ATM cell from the control unit ~~(5)~~ with a correct CRC sum, the management unit ~~(1)~~ resends ~~sends the same~~ an identical ATM cell ~~again, identifying it~~ the ATM cell as a repetition cell; [[-]] when receiving a repetition cell, the control unit ~~(5)~~ checks whether ~~or not~~, following ~~the~~ a first ATM cell, a response ATM cell was transmitted to the management unit ~~(1)~~; and [[-]] if a response ATM cell call was not transmitted to the management unit the control unit ~~no,~~ processes the instructions contained in the cell; or [[-]] if a response ATM cell was transmitted to the management unit the control unit ~~yes,~~ retransmits the response ATM cell which was previously ~~has already been~~ sent once and ~~which has been~~ stored separately, to the management unit ~~(1)~~.

47. (Currently Amended) ~~A~~ The process according to claim 43, ~~characterised in that~~ wherein [[-]] after a specified time limit after sending a first ATM cell addressed to a control unit ~~(5)~~ has lapsed and prior to receiving a response ATM cell from the control unit ~~(5)~~ with a correct CRC sum, the management unit ~~(1)~~ resends ~~sends the same~~ an identical ATM cell ~~again, identifying it~~ the ATM cell as a repetition cell[[; -]], when receiving a repetition cell, the control unit ~~(5)~~ checks whether ~~or not~~, following ~~the~~ a first ATM cell, a response ATM cell was transmitted to the management unit [[(1);]], and [[-]] if a response ATM cell call was not transmitted to the management unit ~~no~~, the control unit processes the instructions contained in the cell[[;]], or [[-]] if a response ATM cell was transmitted to the management unit ~~yes~~, the control unit retransmits the response ATM cell which was previously ~~has already been~~ sent once and ~~which has been~~ stored separately[[,]] to the management unit ~~(1)~~.

48. (Canceled)

49. (Currently Amended) The process ~~according to~~ of claim 2, ~~characterised in that~~ wherein the control unit ~~(5)~~ autonomously and regularly reads in data from devices ~~(4)~~ connected to ~~it~~ the control unit and transmits ~~such~~ the data, integrated into ATM cells, to the management unit ~~(1)~~.

50. (Currently Amended) ~~A~~ The control unit ~~(5) according to~~ of claim 15, ~~characterised in that~~ wherein the management interface ~~(6) corresponds to~~ is the management interface as proposed in Appendix 2 of Utopia Level 2 specification.

51. (Currently Amended) ~~A~~ The management system ~~according to~~ of claim 20, ~~characterised in that~~ wherein the devices ~~(4)~~ comprising registers are ATM interface units of ~~the~~ a physical layer ~~by way of~~ via which ~~the~~ an ATM layer of the ATM network has access to at least one transmission medium.

52. (New) The process of claim 1, wherein said integrating of instructions comprises writing data into the registers of the devices as an operation code.

53. (New) The process of claim 2, wherein said integrating of instructions comprises reading data from the registers of the devices as an operation code.

54. (New) The ATM cell of claim 23, wherein said extraction of individual instructions associated with the particular device comprises at least one of writing register data into the devices or reading register data from the devices.

55. (New) The ATM cell of claim 23, wherein the cell type is new cell or a retransmitted cell.

56. (New) The method of claim 27, wherein said extraction of individual instructions associated with the particular device comprises at least one of writing register data into the devices or reading register data from the devices.

57. (New) The management unit of claim 31, wherein said extraction of individual instructions associated with the particular device comprises at least one of writing register data into the devices or reading register data from the devices.

58. (New) The management unit of claim 31, wherein the cell type is new cell or a retransmitted cell.

59. (New) The control unit of claim 14, wherein said extraction and performance of the individual instructions comprises at least one of writing register data into the device and reading register data from the devices.